ABSTRACT OF THE DISCLOSURE

An integrated circuit includes a plurality of processing stages each including processing logic 1014, a non-delayed signal-capture element 1016, a delayed signal-capture element 1018 and a comparator 1024. The non-delayed signal-capture element 1016 captures an output from the processing logic 1014 at a non-delayed capture time. At a later delayed capture time, the delayed signal-capture element 1018 also captures a value from the processing logic 1014. An error detection circuit 1026 and error correction circuit 1028 detect and correct random errors in the delayed value and supplies an error-checked delayed value to the comparator 1024. The comparator 1024 compares the error-checked delayed value and the non-delayed value and if they are not equal this indicates that the non-delayed value was captured too soon and should be replaced by the error-checked delayed value. The non-delayed value is passed to the subsequent processing stage immediately following its capture and accordingly error recovery mechanisms are used to suppress the erroneous processing which has occurred by the subsequent processing stages, such as gating the clock and allowing the correct signal values to propagate through the subsequent processing logic before restarting the clock. The operating parameters of the integrated circuit, such as the clock frequency, the operating voltage, the body biased voltage, temperature and the like are adjusted so as to maintain a finite non-zero error rate in a manner that increases overall performance.

[Figure 14]